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Article in *IEEE Electron Device Letters* · August 2007

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# Metamorphic Heterostructure InP/GaAsSb/InP HBTs on GaAs Substrates by MOCVD

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**Abstract**—Good-quality metamorphic InP buffer layers have been successfully grown on GaAs substrates by metal–organic chemical vapor deposition. Characterization by atomic force microscope, transmission electron microscopy, high-resolution X-ray diffraction, and Hall measurements indicated that the layers are of high crystalline quality, good mobility, and excellent surface morphology. On this buffer, we demonstrated the first metamorphic InP/GaAsSb/InP double heterojunction bipolar transistors (DHBTs) with good material quality and device performance. Metamorphic DHBTs showed direct-current and radio-frequency characteristics that are comparable to those grown on lattice-matched InP substrates.

**Index Terms**—Double heterojunction bipolar transistor (DHBT), GaAs substrate, InP/GaAsSb/InP, metamorphic buffer.

## I. INTRODUCTION

**I**nP-BASED DOUBLE heterojunction bipolar transistors (DHBTs) have wide applications in high-frequency communication systems. Among them, InP/GaAsSb/InP DHBT has a unique Type-II heterostructure and was shown to exhibit low turn-on voltage and high-speed performance [1]. To combine the advantages of GaAs substrates with the benefits of high-performance InP-based devices, metamorphic technology is one of the promising solutions for commercialization of InP-based devices and circuits. Metamorphic heterojunction bipolar transistor (MHBT) structures that are grown by molecular beam epitaxy (MBE) have been reported by a few groups, with reported device performance that is nearly comparable to that on InP substrates [2]. However, despite the success of heterojunction bipolar transistor (HBT) manufactured by metal–organic chemical vapor deposition (MOCVD) technology, there has

been extremely few reports on MHBT by MOCVD [3]. The large lattice mismatch (4%) between InP and GaAs lattices makes the heteroepitaxy very difficult, and the requirements of metamorphic HBT device structures are stringent.

Even though much effort has been made to grow metamorphic InP directly on GaAs substrates by MOCVD [4], [5], it is not until recently that Liao *et al.* [7] have shown good material results with high mobility and decent surface morphology, using low-temperature metamorphic growth. A two-step method using low-temperature InP as the nucleation layer, followed by a thick InP layer at high temperatures, is preferable [7]–[9]. Horikawa *et al.* [8] have shown InP buffer layers with good mobility using the two-step method. To smooth the wavy patterned surface, a thick InP layer ( $> 2 \mu\text{m}$ ) was needed to obtain high crystalline quality, relieving the remaining stress in the layer and reducing the threading dislocation density. In our work, a 120-nm-thick low-temperature InP nucleation layer was found to be effective in reducing stress in the subsequent metamorphic InP layer (600 nm) growth on GaAs substrates at typical high epitaxial growth temperatures. This high-quality composite buffer layer allowed the growth of the first Sb-based MHBTs using MOCVD. An *in-situ* optical reflectance signal was used to monitor the crystalline quality and surface morphology during the metamorphic growth.

## II. GROWTH AND DEVICE FABRICATION

Metamorphic InP films with DHBT structure were grown on GaAs substrates in a low-pressure MOCVD system (Aixtron 200/4); Trimethylindium (TMI) and phosphine ( $\text{PH}_3$ ) were used as precursor sources, with hydrogen as the carrier gas, and 4-in (100) GaAs wafers with  $2^\circ$  off toward (111) were used as substrates. To initiate on the GaAs substrate, a 30-nm GaAs layer [7] was grown first at  $500^\circ\text{C}$ , followed by an InP nucleation layer that is deposited at  $450^\circ\text{C}$  with a V/III ratio of 120, to relieve the stress that resulted from lattice mismatch. This was followed by growing a high-temperature InP layer at  $600^\circ\text{C}$ – $650^\circ\text{C}$  with a V/III ratio of 230. It was reported that the range of V/III ratio selection for the nucleation layer is very important [6]. Both a low V/III ratio [9] of about 20 and high V/III ratios [5], [7] of up to 500 were reported to be suitable for the InP nucleation layer growth. In our growth studies, a V/III ratio of 120 was our optimal condition. We found that V/III ratios of greater than 250 would degrade the surface, while a ratio between 60 and 150 would result in the best surface morphology.

Manuscript received January 23, 2007; revised April 5, 2007. This work was supported in part by the Innovation and Technology Commission of Hong Kong under Grant ITS176/01B and in part by the Research Grants Council of Hong Kong under CERG Grant HKUST6249/02E and Grant 615506. The work of Y. Zeng, H. G. Liu, N. G. Tao, and C. R. Bolognesi was supported by the Natural Sciences and Engineering Research Council of Canada. The review of this letter was arranged by Editor J. del Alamo.

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Digital Object Identifier 10.1109/LED.2007.899455

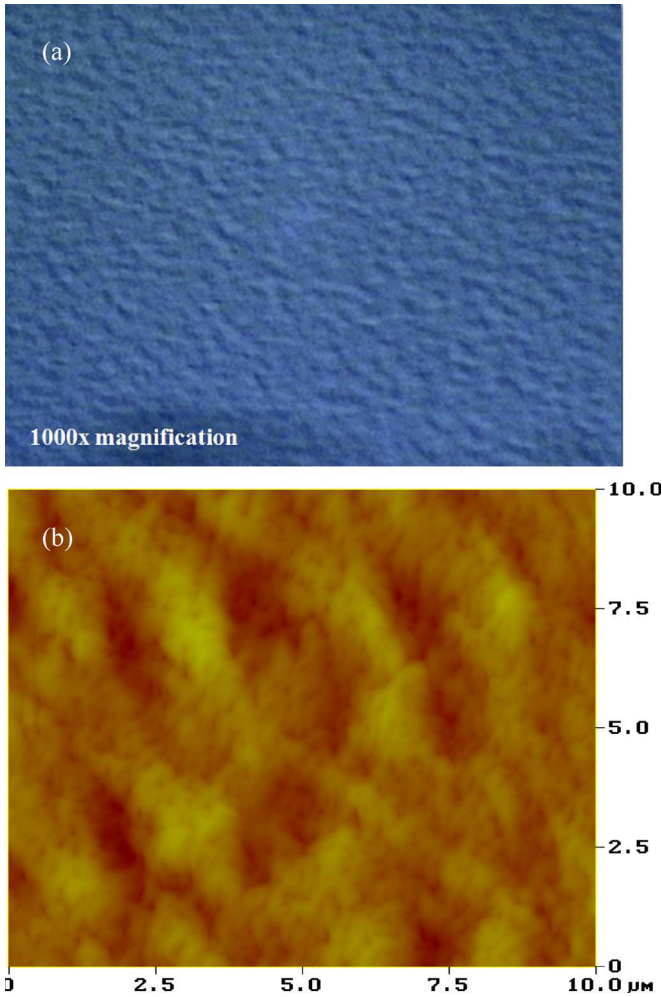


Fig. 1. (a) Micrograph (1000 $\times$ ) of the InP layer surface. (b) Surface roughness of 5.0 nm (rms) that is measured by AFM.

The concept of thin nucleation layers (20–50 nm) was used in previously reported work [5]–[10]. However, very few showed good surface morphology with low defect density [7] that is suitable for device applications. Thick ( $> 1 \mu\text{m}$ ) high-temperature InP overgrown layers were necessary to improve the crystalline quality. In our study, 120 nm was determined to be the optimum thickness for the nucleation layer, whose Raman spectrum showed the sharpest peak and highest intensity, indicating the best crystalline quality as compared to thinner or thicker layers. On top of this optimized nucleation layer, a relatively thin high-temperature InP layer (only 600 nm thick) provided sufficiently high quality as the buffer layer for device growth. Optical microscopy showed uniform and specular surfaces with fine texture [Fig. 1(a)]. Atomic force microscope (AFM) surface roughness measurement resulted in an rms of 5.0 nm over a  $10 \times 10 \mu\text{m}^2$  scan [Fig. 1(b)], which is by far the smoothest for metamorphic growth by MOCVD. The full-width at half-maximum of the X-ray diffraction rocking curve was 332 arcsec for the 600-nm InP layer and was further reduced to 300 arcsec for a 2.5- $\mu\text{m}$  InP layer.

The best Hall mobility that was determined by van der Pauw geometry was  $2800 \text{ cm}^2/\text{V} \cdot \text{s}$  with a carrier concentration of  $8 \times 10^{15} \text{ cm}^{-3}$  at room temperature and  $4000 \text{ cm}^2/\text{V} \cdot \text{s}$  with a

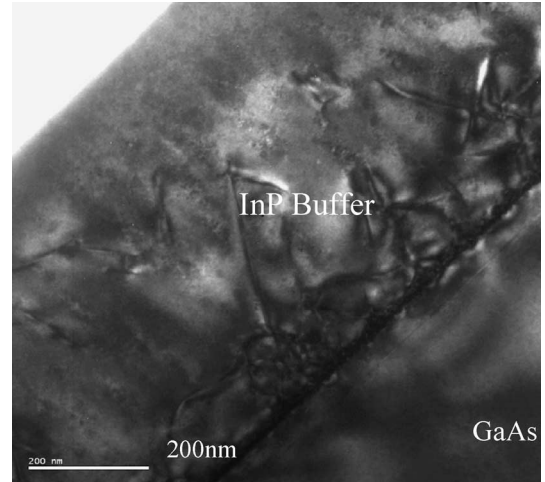


Fig. 2. TEM result of the InP buffer layer.

TABLE I  
DEVICE STRUCTURE OF MHB T

Layer	Material	Nominal Doping	Thickness (nm)
Emitter cap	InGaAs	$10^{19}$ : Si	100
N <sup>+</sup> emitter	InP	$10^{19}$ : Si	50
N <sup>-</sup> emitter	InP	$10^{17}$ : Si	50
Base	GaAs <sub>0.55</sub> Sb <sub>0.45</sub>	$3 \times 10^{19}$ : C	50
Collector	InP	$10^{16}$ : Si	200
Sub-collector	InGaAs	$8 \times 10^{18}$ : Si	300
~ 600nm InP metamorphic buffer			
S.I. GaAs substrate			

carrier concentration of  $2.0 \times 10^{15} \text{ cm}^{-3}$  at 77 K. The density of threading dislocations was determined to be  $7 \times 10^7 \text{ cm}^{-2}$  from transmission electron microscopy (TEM) measurements (Fig. 2).

InP/GaAsSb/InP DHBT structures, as shown in Table I, were subsequently grown on the preceding optimized buffer. The C-doped GaAsSb base layer has an average sheet resistance of about  $1100 \Omega/\square$  that is determined by the transmission-line matrix method. The hole carrier concentration and the average mobility are  $3 \times 10^{19} \text{ cm}^{-3}$  and  $30 \text{ cm}^2/\text{V} \cdot \text{s}$ , respectively. All metamorphic transistors were fabricated by the Compound Semiconductor Device Laboratory at Simon Fraser University.

Triple mesa emitter-up MHB T s were fabricated by standard contact alignment and selective wet etching. For the small area devices, the self-aligned base process was used.

Ti/Pt/Au was used for emitter and collector ohmic contacts, and Pt/Ni/Pt/Au was used for the base ohmic contact. The typical undercuts of the emitter and base contacts were 0.15 and 0.75  $\mu\text{m}$  on each side, respectively. Large devices have emitter areas ranging from  $80 \times 80 \mu\text{m}^2$  to  $20 \times 30 \mu\text{m}^2$ , and small devices have a nominal  $1 \times 24 \mu\text{m}^2$  emitter area. The active region of the device was isolated from the probing pads by air-bridges. No passivation was done on the devices.

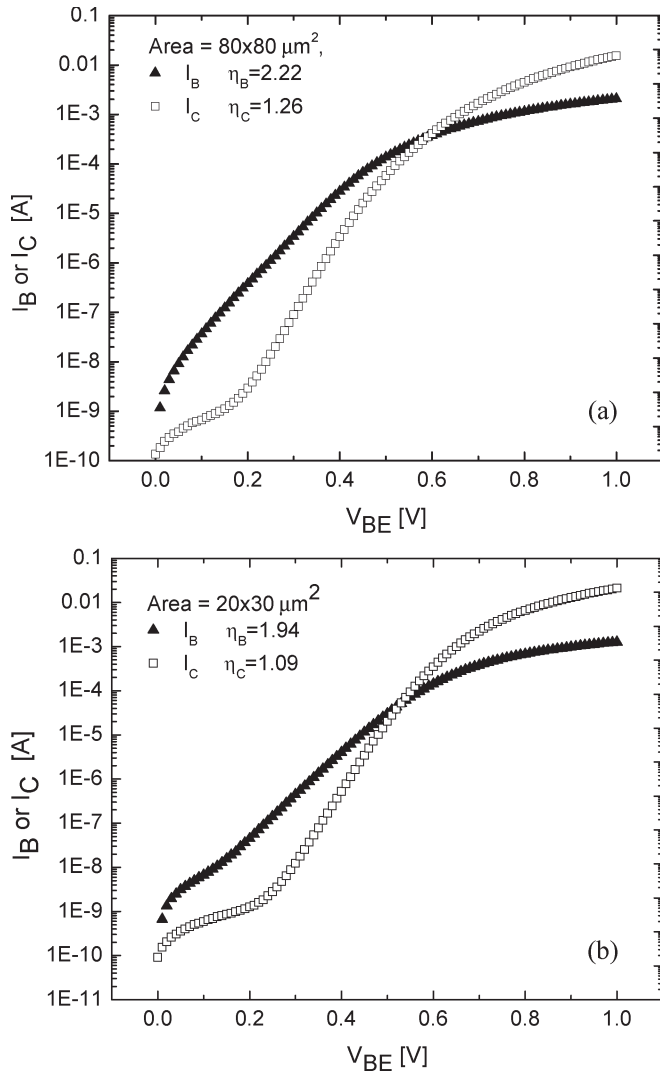


Fig. 3. (a) Gummel plot of large-area device with  $80 \times 80 \mu\text{m}^2$  emitter area. (b) Gummel plot of a smaller area device with a  $20 \times 30 \mu\text{m}^2$  BE junction.

### III. TRANSISTOR CHARACTERIZATION

Fig. 3(a) and (b) show the Gummel plots of two large-area devices. The ideality factor of the collector current for the smaller device is comparable to the MOCVD-grown HBTs on InP substrates [1] and the MBE-grown MHBTs [2]. The high ideality factors (2.22 and 1.94) of the base currents indicate that the carrier recombination at the base region and/or BE junction may be serious. This is probably due to a significant amount of defects in the base and less than ideal BE interface.

Fig. 3 also shows that the ideality factors of both base and collector currents increase with the emitter size. This further indicates that the ideality factor may be related to the quality of the metamorphic material and interfaces because larger-area devices are likely to have more defects. The reverse B/C diode current was below or in the nanoampere range, for  $1 \times 24 \mu\text{m}^2$  MHBTs. The common-emitter current gain  $\beta$  of these devices can be as high as 20.

Fig. 4(a) shows the common-emitter characteristics of a typical MHBT. Low collector leakage current ( $I_{\text{CEO}} < 1 \mu\text{A}$  at  $V_{\text{CE}} = 1 \text{ V}$ ) and a small offset voltage (25 mV) can be

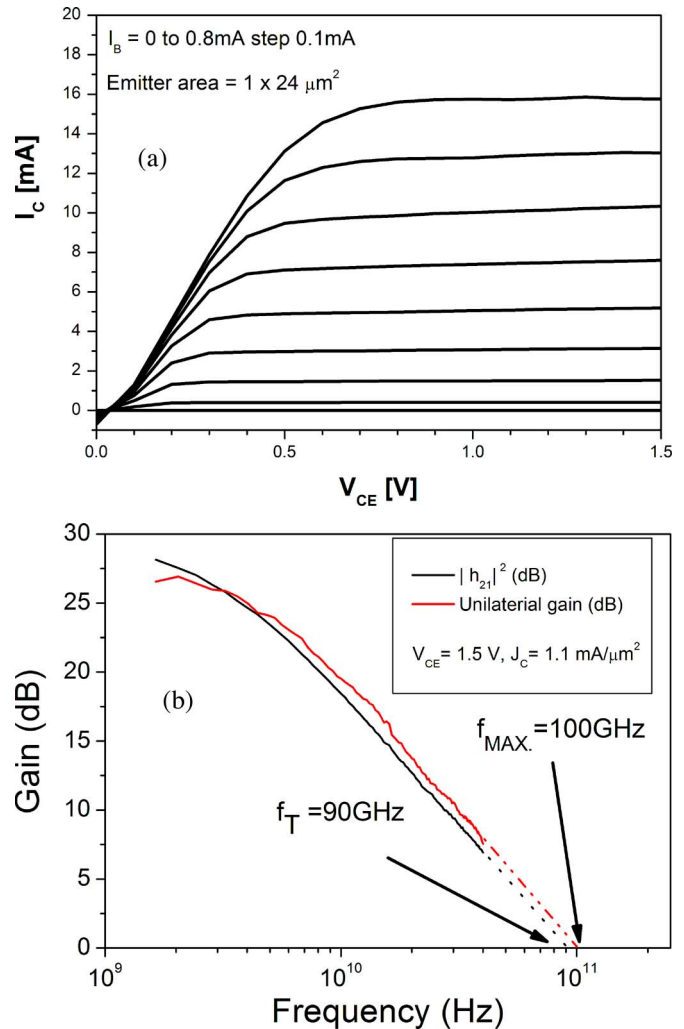


Fig. 4. (a) Common-emitter characteristics of a small emitter area device. (b) Unilateral and current gains of a  $1 \times 24 \mu\text{m}^2$  MHBT.

observed. The maximum transconductance is 24 mS. The measured  $BV_{\text{CEO}}$  of the large- and small-area devices is over 8.5 and 7.3 V, which might be attributed to the relatively low electron multiplication coefficient in the InP collector layer [1]. The breakdown voltage usually increases as in smaller devices on the InP substrate [1], but our metamorphic device features the opposite trend, i.e., slightly lower breakdown voltages are found in smaller devices. The exact reason for this is not known, but it probably involves defects such as threading dislocations in the metamorphic buffer. Fig. 4(b) shows the RF unilateral and current gains of the MHBT. A  $f_T = 90 \text{ GHz}$  and  $f_{\text{MAX}} = 100 \text{ GHz}$  have been demonstrated for the  $1 \times 24 \mu\text{m}^2$  emitter device.

### IV. CONCLUSION

Growth conditions for the nucleation InP layer were optimized for metamorphic growth of InP-based devices on GaAs substrates. From our results, a thickness of 120 nm and a V/III ratio of about 120 were found to be the best for stress relief and surface morphology. With the improved metamorphic InP buffer layer, the first metamorphic InP/GaAsSb/InP HBT was

fabricated. The direct-current and RF characteristics of the devices show that GaAsSb-based HBTs can be successfully grown on GaAs substrates by MOCVD, demonstrating the advantages of both GaAsSb-based DHBTs and metamorphic growth. Further development is required to optimize device performance, particularly, with respect to the emitter–base junction.

#### ACKNOWLEDGMENT

The authors would like to thank Rohm and Haas Electronic Materials LLC for their support of metal–organic materials.

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